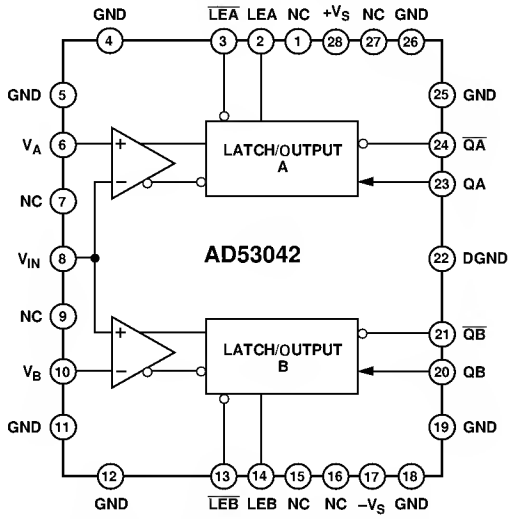
High Speed Window Comparator

AD53042

FEATURES
–2 V to +7 V Input Voltage Range
Low V_{IN} Bias Current (<100 nA)
Up to 5 V/ns Input Signal Tracking
Low Dispersion of ±100 ps
28-Lead PLCC Package

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems

FUNCTIONAL BLOCK DIAGRAM



NOTE:
NOT THE ACTUAL PHYSICAL LAYOUT OF DEVICE.
NC = NO CONNECTION INSIDE PACKAGE.

PRODUCT DESCRIPTION

The AD53042 is an ultrahigh speed window comparator with latch. It uses a high speed monolithic process to provide high dc accuracy without sacrificing input voltage range. On-chip connection of the common input eliminates the contributions of a second bonding pad and package pin to the input capacitance, resulting in a maximum input capacitance of 2 pF.

The AD53042 employs a high precision differential input stage with a common mode range of 9 V. Its complementary digital outputs are fully ECL compatible. The output stage is capable of driving a 50 Ω line terminated to –2 V. The device also provides a latch function, allowing operation in track-hold mode and can also be used to generate hysteresis.

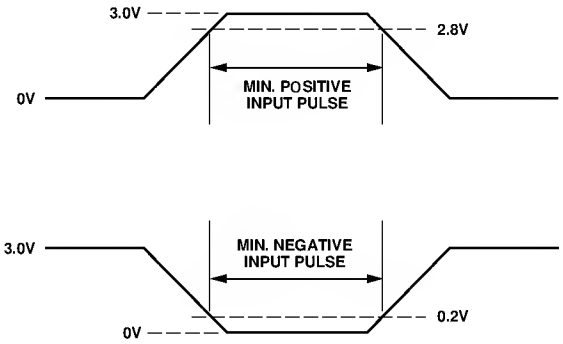


Figure 1. Typical Application Circuit

REV. 0

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AD53042– SPECIFICATIONS

(All specifications apply with T_C = 40°C to 100°C and $+V_S$ = +7.75 V to +11.5 V; $-V_S$ = – 3.95 V to – 7.7 V unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions
POWER SUPPLIES					
I –Positive Supply Currents			65	mA	No Load
I –Negative Supply Current	–85			mA	No Load
P –Power Dissipation			1.19	W	No Load, $+V_S$ = +10 V, $-V_S$ = –5.2 V
DC INPUT CHARACTERISTICS					
Offset Voltage (V_{OS})	–10		10	mV	CMV = 0 V
V_{IN} Bias Current	–0.5	<0.1>	0.5	µA	V_{IN} = 0 V
V_A, V_B Bias Current	–20		20	µA	V_{IN} = 0 V
Capacitance V_{IN}, V_A, V_B			2	pF	
Voltage Range (V_{CM})	$-V_S$ + 2.7		$+V_S$ – 2.5	V	
Differential Voltage (V_{DIFF})			9	V	
Nonlinearity	–5		5	mV	See Note 1
V_A/V_B Interaction			0.1	mV/V	
BIAS CURRENT					
Change vs. Comparator State	–1		1	µA	
Nonlinearity	–2		2	µA	
Tempco		±0.1		µA/°C	
LATCH ENABLE INPUTS					
Common-Mode Range	–2		1	V	
Differential Voltage	0.4		3	V	
Logic "1" Current (L_{IH})			200	µA	
Logic "0" Current (L_{IL})	–10			µA	
DIGITAL OUTPUTS					
Logic "1" Voltage (V_{OH})	–0.98			V	Q or $\overline{Q}$, 50 Ω to –2 V
Logic "0" Voltage (V_{OL})			–1.5	V	Q or $\overline{Q}$, 50 Ω to –2 V
SWITCHING PERFORMANCE					
Propagation Delay					
Input to Output			2	ns	V_{IN} = 2 V p-p, t_{PDR}, t_{PDF}, Figure 1, Note 2
Part-to-Part Skew			1	ns	
Change vs. Temperature		±1		ps/°C	
DISPERSION					
5 V p-p Input (All Edges)		±100		ps	10%, 90% 0.5 V/ns, 3 V/ns
5 V p-p Input (All Edges)		±175		ps	10%, 90% 5 V/ns
V Slew = 1 V/ns (All Edges)		±50		ps	10%, 90% 3 V, 5 V
V Slew = 1 V/ns (All Edges)		±50		ps	20%, 80% 1 V
Minimum Pulsewidth		<1		ns	See Note 3
Edge Interaction		<200		ps	See Note 4
Duty Ratio		<100		ps	See Note 5
Comparator Interaction		<100		ps	

NOTES

[1]Defined as change in V_{OS} from $-V_S$ + 2.95 V to $+V_S$ – 2.75 V (throughout the range) after V_A and V_B are corrected for gain and offset using 0 V and 5 V.

[2]Propagation delay is measured from the input threshold crossing at the 50% point of a 0 V to 5 V input to the output Q and $\overline{Q}$ crossing.

[3]The minimum input pulsewidth that will maintain a 600 mV ECL swing on the output. The input is a 0 V to 3 V signal with a 3 V/ns rise and fall times. The input pulsewidth is measured between the 2.8 V point of a positive input pulse and the 0.2 V of a negative input pulse. See Figure 2.

[4]Maximum Change in propagation delay as the input pulse is reduced from 50 ns to a 2 ns pulsewidth. 0 V to 3 V swing with 3 V/ns rise/fall time and 25% duty cycle.

[5]Maximum Change in propagation delay as the input pulse is reduced from 99% to a 1% duty cycle. 0 V to 3 V swing with 3 V/ns rise/fall time and 50 ns to 4.95 µs pulsewidth, period = 5 µs.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND ..... +12 V
- $-V_S$ to GND ..... –8 V
- $+V_S$ to $-V_S$ ..... +17 V

Inputs
- V_{IN}, V, $\overline{V}$ ..... $+V_S$ – 13.5 V, $-V_S$ + 13.7 V
- LEA, $\overline{LEA}$, LEB, $\overline{LEB}$ ..... $+V_S$ – 14 V, $-V_S$ + 10 V

Currents
- I ($+V_S$) ..... 95 mA
- I ($-V_S$) ..... –75 mA
- QA, $\overline{QA}$, QB, $\overline{QB}$ ..... –40 mA to +2 mA

Environmental
- Operating Temperature (Ambient) ..... 0°C to +70°C
- Storage Temperature ..... –65°C to +125°C
- Lead Temperature (Soldering, 20 sec) ..... +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The device must suffer no reliability degradation if any supply pin is either shorted to ground or left floating for an indefinite periods of time during normal operation.

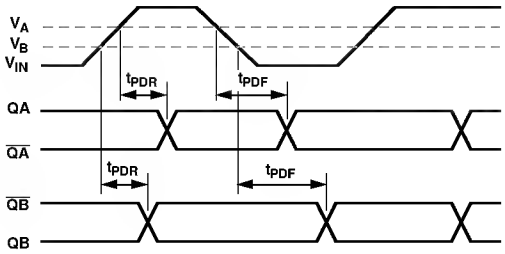
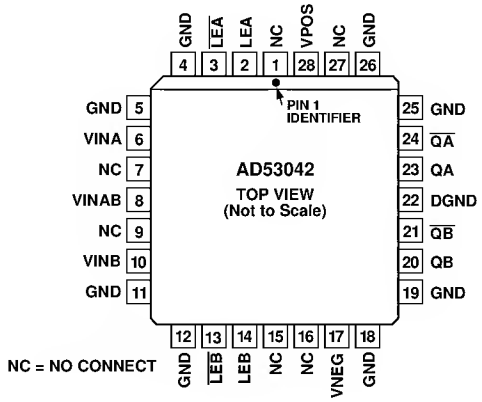


Figure 2. Timing Diagram

ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity Per Shipping Container	Package Option
AD53042KRP	28-Lead PLCC	Tube, 36 Pieces	P-28A

PIN CONFIGURATION



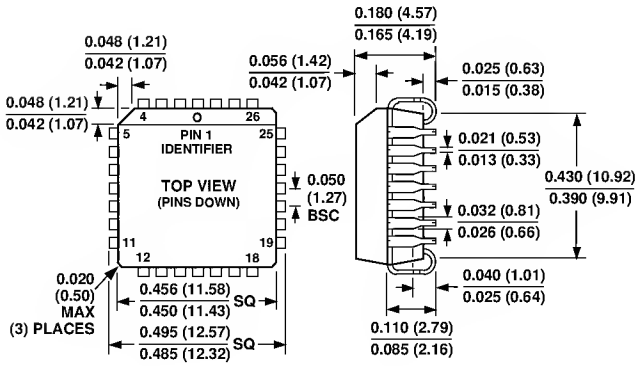
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53042 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Plastic Leaded Chip Carrier (P-28A)



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